CLAIMS

What is claimed is:

1. A semiconductor device comprising:

a substrate having a surface orientation of (100);

a gate electrode formed on the substrate;

a Slim spacer formed on the top of the substrate

source-to-drain axis is formed along the <100>

2. The semiconductor device of claim 1, wherein the width of the Slim spacer is less than about 500 Angstroms.

3. The semiconductor device of claim 1, wherein the polysilicon gate structure comprises a gate length of less than about 80 nanometers.

4. The semiconductor device of claim 1, forming at least one dielectric layer over the polysilicon gate structure and spacers in tensile stress.

5. The semiconductor device of claim 4, wherein the tensile-stress film exerts a tensile stress of a magnitude of about 50 MPa to about 2 GPa.

6. A method for forming a Slim spacer adjacent a CMOS gate structure comprising the steps of:

providing a semiconductor substrate comprising a gate structure including at least one overlying hardmask layer;

forming dielectric spacers adjacent the gate structure;

carrying out an ion implant process;

carrying out at least one of a wet and dry etching process to reduce the width of the spacers; and,

forming at least one dielectric layer over the gate structure and spacers in one of tensile and compressive stress to form a stress level in a channel region.

7. The method of claim 1, wherein dielectric layer comprises compressive stress to enhance PMON drive current.

8. The method of claim 1, wherein dielectric layer comprises tensile stress to enhance NMON drive current.

9. The method of claim 1, wherein dielectric layer comprises tensile stress to enhance NMON drive current.

10. The method of claim 1, further comprising forming salicides adjacent the spacers and over the polysilicon gate structure prior to the step of forming at least one dielectric layer.

11. The method of claim 1, wherein the width of the spacers is reduced by an amount greater than about 20 percent.

12. The method of claim 1, wherein the width of the spacers is reduced to have a final width less than about 500 Angstroms.

13. The method of claim 1, wherein the width of the spacers is reduced to have a final width less than about 400 Angstroms.

14. The method of claim 1, wherein the polysilicon gate structure comprises a gate length of less than about 80 nanometers.

15. The method of claim 1, further comprising the step of annealing the polysilicon gate structure to recrystallize amorphous portions and increase one of a compressive and tensile stress in the channel region.

16. The method of claim 7, wherein the at least one dielectric layer is removed to leave an increased stress level in the channel region.

17. The method of claim 1, wherein the oxide comprises silicon oxide formed by a CVD process.

18. The method of claim 1, wherein the nitride is selected from the group consisting of silicon nitride and silicon oxynitride formed by a CVD process.

19. The method of claim 1 wherein the at least one hardmask layer comprises a lowermost oxide layer and an uppermost nitride layer.

20. The method of claim 1, wherein the at least one dielectric layer is selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, and silicon oxycarbide.

21. A CMOS structure having a reduced S/D electrical resistance and increased charge carrier mobility in a channel region comprising:

a semiconductor substrate;

a gate structure formed overlying the semiconductor substrate comprising a polysilicon electrode;

spacers adjacent either side of the polysilicon electrode comprising an oxide/nitride portion adjacent the polysilicon electrode; and,

wherein source/drain extension (SDE) regions comprising the semiconductor substrate extend beyond a maximum width of the spacers.

22. The CMOS structure of claim 25, further comprising at least one dielectric layer in one of tensile and compressive stress overlying the gate structure and spacers.

23. The CMOS structure of claim 26, wherein the at least one dielectric layer is selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, and silicon oxycarbide.

24. The CMOS structure of claim 25, further comprising salicide portions comprising a portion of the SDE doped regions.

25. The CMOS structure of claim 25, wherein the gate length is less than about 80 nm.

26. The CMOS structure of claim 25, wherein the maximum width of the spacers is less than about 500 Angstroms.

27. The CMOS structure of claim 25, wherein the maximum width of the spacers is less than about 400 Angstroms.

28. The CMOS structure of claim 25, wherein the oxide portion comprises CVD silicon oxide.

29. The CMOS structure of claim 25, wherein the nitride portion is selected from the group consisting of CVD silicon nitride and CVD silicon oxynitride.

30. The CMOS structure of claim 25, wherein the spacers comprises substantially vertical sidewalls.

31. A CMOS structure having a reduced S/D electrical resistance and increased charge carrier mobility in a channel region comprising:

a semiconductor substrate;

a gate structure overlying the semiconductor substrate comprising a polysilicon electrode;

spacers adjacent either side of the polysilicon electrode comprising an oxide portion adjacent the polysilicon electrode and a nitride portion adjacent the oxide portion;

wherein a maximum width of the spacers is such that a portion of underlying source/drain extension (SDE) doped regions in the semiconductor substrate are exposed; and,

salicide portions extending into a portion of the SDE doped regions.

32. The CMOS structure of claim 35, further comprising at least one dielectric layer overlying the gate structure and spacers in one of tensile and compressive stress.

33. The CMOS structure of claim 36, wherein the at least one dielectric layer is selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, and silicon oxycarbide.

34. The CMOS structure of claim 35, wherein the gate length is less than about 80 nm.

35. The CMOS structure of claim 35, wherein the maximum width of the spacers is less than about 500 Angstroms.

36. The CMOS structure of claim 35, wherein the maximum width of the spacers is less than about 400 Angstroms.

37. The CMOS structure of claim 35, wherein the oxide portion comprises CVD silicon oxide.

38. The CMOS structure of claim 35, wherein the nitride portion is selected from the group consisting of CVD silicon nitride and CVD silicon oxynitride.

39. The CMOS structure of claim 35, wherein the spacers comprises substantially vertical sidewalls.